A method for handling data between a clock and data recovery circuit and a data processing unit of a telecommunications network node of an asynchronous network, as well as a bit rate adaptation circuit and a clock and data recovery system.

Background of the Invention

The invention relates to a method for handling data between a clock and data recovery circuit and a data processing unit of a telecommunications network node of an asynchronous network, and to a bit rate adaptation circuit, a clock and data recovery system and a telecommunications network node which implement said method.

Typically, network node elements of communication networks structurally comprise an input port, a Clock and Data Recovery circuit, a bit rate adaptation system, a data processing system and an output port. The Clock and Data Recovery circuit, in charge of regenerating the data received at the input port and the clock at which this data was transmitted throughout the network, passes these two signals to a bit rate adaptation system which is in charge of transmitting the recovered data to the node processing stage (switching/routing) at a rate which is indicated by the local clock of the network node.

Within network node elements dedicated to synchronous transport (e.g. SDH/SONET), such bit rate adaptation systems comprise usually a first-in-first-out (FIFO) memory with read and write pointers which are controlled by two independent clocks, a local network node clock and a recovered data clock taken out from the input signals, respectively.

In synchronous networks, such as SDH/SONET, clock generation and distribution can be well controlled, as data signal timing is related to a single timing reference (i.e. global reference). Incoming data frames to the network node are written onto

and read from the memory stack in a synchronous manner, that is, read and write pointers are triggered with independent clocks which run continuously and more or less synchronously. In US Patent 6,166,963 for example, a system is disclosed which comprises a FIFO memory stack, a write unit, a read unit and a first and a second synchronization circuit. The write unit is configured to add elements to the FIFO memory stack based upon a first clock domain, and the read unit is configured to read elements from the FIFO stack based upon a second clock domain. The first synchronization circuit is operationally coupled with the write unit and is configured to receive the write pointer and synchronize it to the second clock domain. The second synchronization circuit is operationally coupled with the read unit and is configured to receive the read pointer and synchronize it to the first clock domain.

On the other hand, new type of asynchronous networks introduce new requirements for network node internal subsystems. US Patent 6,278,718 although suited for another type of asynchronous communication, more specifically, distributed asynchronous networks, is seen as the closest state of the art concerning the present invention.

Summary of the Invention

We define here an asynchronous network as one in which the network nodes do not share global synchronization at the bit level. Instead, each node operates with independent bit level clocks, that is, in each node, the bit level clock (or local clock, used to drive the subsystems within the node) operates at a standardized nominal bit rate, but there is no attempt made to achieve phase synchronization between bit-level clocks in different nodes. The physical optical transmission across the network occurs in burst mode, where a "burst" is a finite contiguous string of bits in a standardized signal format and may represent an individual packet or cell (with header and payload). Routing across the network could be

achieved by any appropriate method, such as circuit switching, packet or cell switching, self-routing, etc.

In this type of networks, the incoming data frames begin with a bit synchronization field including a synchronization sequence with bit level changes, which is used by the Clock and Data Recovery circuit to produce the recovered clock output and regenerate the data signal, but in contrast to the synchronous transport frames, they come with an associated gap or guard band of variable length which does not include reference data and is composed of a constant "0" or constant "1" bit level. During this gap time then, because the needed bit level changes on the data signal are missing, the recovered clock will not be generated, the bit rate adaptation system will not trigger the write process and thus no data is written into the memory stack. Meanwhile the local clock, which triggers the read process, will run continuously during this time and read information from the memory.

We see then that the use in this case of traditional circuits as the ones described above for synchronous transmission would result in a misalignment of the read and write processes and consequently the passing of erroneous information to the data processing stage of the node.

Accordingly an improved system and method for data handling is needed, and more specifically a bit rate adaptation system which avoids the misalignment of the read and write processes.

An improved system and method for the handling of data between a Clock and Data Recovery circuit and a data processing unit of an asynchronous communications network node is herein provided to avoid passing of erroneous data to said data processing stage.

The object is achieved according to the invention by a method for handling data between a Clock and Data Recovery circuit and a processing unit of a telecommunications network node of an asynchronous network according to claim 1, a bit rate adaptation circuit according to claim 2, a Clock and Data Recovery system according to claim 3 and a telecommunications network node according to claim 4.

The present invention is not restricted to a FIFO-based method or system. It can be applied to any common memory unit, such as a transfer buffer or queue, through which the data are transferred from one entity to another.

Brief Description of the Drawings

Advantageous configurations of the invention emerge from the dependent claims, the following description and the drawings.

An embodiment example of the invention is now explained with the aid of Figures 1 to 4.

Fig. 1 shows a high level block diagram of a telecommunications network node of an asynchronous network according to the invention.

Fig. 2 shows the data structure received by the telecommunications network node according to the invention and the timing diagram of the recovered and local clock of said node.

Fig. 3 shows a block diagram of the bit rate adaptation system of the telecommunications network node according to the invention.

Fig. 4 shows a more detailed block diagram of the bit rate adaptation circuit of figure 3.

Detailed Description of the Drawings

Fig. 1 shows a high level block diagram of a telecommunications network node of an asynchronous network TNN, comprising an input port IPx, a Clock and Data Recovery circuit CDR, a Bit Rate Adaptation circuit, often called Bit Rate Adaptation system BAS, according to the present invention, a Data Processing system DP and an output port OPy.

The input port IPx is connected to the Clock and Data Recovery circuit CDR, said circuit CDR passing the recovered data at incoming bit rate Dlb1 and the recovered clock Rclk to the Bit Rate Adaptation circuit BAS, which adapts data to the local bit rate using a local clock Lclk as a reference, according to the invention, this data Dlb2 being passed to the Data Processing unit DP for Switching or Routing operations and being transmitted to the network through the output port OPy.

Fig. 2 shows the data structure DS received by the telecommunications network node TNN of an asynchronous network according to the invention at the input port IPx and the timing diagram of the recovered Rclk and local clock Lclk of said node.

Each data frame packet F comprises a bit synchronization field BSy, a header field H and a payload field P. A guard band G between frames F which does not contain valid data and bit level changes and whose length or duration is variable,

is used to maintain proper separation of frames F and to allow time for the operation of routing switches.

When a new data frame F is received at the node, the Clock and Data Recovery circuit CDR will detect the bit synchronization field BSy and from the bit level changes of the data it will adapt its recovered clock Rclk output to the incoming data frequency and phase. During the guard band G duration, because no level changes exist, no recovered clock Rclk will be generated. On the other hand, it can also be seen in the figure that the local clock Lclk runs continuously.

Fig. 3 shows the preferred embodiment of the Bit Rate Adaptation circuit BAS of a telecommunications network node according to the invention, which comprises a memory unit MEM and a Pointer Synchronization Controller PSC.

Asynchronous data in the form of frames F arrive on data input line DIb1 and are written into the memory unit MEM with a clock controlled by the recovered clock input Rclk. A local clock Lclk input controls the reading of data from the memory unit MEM which appears on the data output line DIb2.

The Pointer Synchronization Controller PSC monitors the frames F present in the input data line DIb1, receives as input the recovered clock Rclk and the local clock Lclk, and monitors/controls the addresses of the Read and Write Pointers via the monitor/control line M/C.

In Fig. 4 is schematically shown the detailed construction of a preferred embodiment of the Bit Rate Adaptation circuit BAS according to the invention, comprising the memory unit MEM with a memory stack MS, a write process circuit Wp and a read process circuit Rp, and a Pointer Synchronization Controller PSC.

The Bit Rate Adaptation circuit BAS has a recovered data input DIb1 connected to the memory stack MS and the Pointer Synchronization Controller PSC; a recovered clock input Rclk connected to the write process circuit Wp and the Pointer Synchronization Controller PSC; and a local clock input Lclk connected the read process circuit Rp and the Pointer Synchronization Controller PSC. The data output DIb2 of the Bit Rate Adaptation circuit BAS being the output of the memory stack MS, and the Pointer Synchronization Controller PSC being also connected to the read Rp and write process circuit Wp, which are connected to the memory stack MS.

Data frame F elements are stored on a stack MS in a manner so that the oldest elements are removed first. One process may add elements to the stack MS, called write process, and another may remove elements from the stack MS and pass them to the next processing system, called read process. The write process circuit Wp must maintain an address pointer, called write pointer Wptr, so that it can add elements to the stack MS. Similarly, the read process circuit Rp must maintain an address pointer, called read pointer Rptr, so that it can remove elements from the stack MS. The write process circuit Wp generates the write pointer Wptr in the recovered clock Rclk domain and the read process circuit Rp generates the read pointer Rptr in the local clock Lclk domain.

An additional Pointer Synchronization Controller PSC circuitry will control the right alignment of both memory address pointers and thus avoiding passing wrong data information to the next stage following the bit adaptation system.

Initially, the write process Wp begins by storing an element at a fixed memory stack MS location. The write process Rp then adds frame F elements at sequential memory locations by incrementing the write pointer Wptr at a rate indicated by the recovered clock Rclk. When the end of the data frame F has been reached and the pointer synchronization controller PSC detects a guard band G, it will set the write pointer, by means of a set command SWc and a write address set signal

SWptr, to a fixed address value(e.g. "0"), which will be starting address for storing the header H and payload P field elements of the data frame F in the memory stack MS.

The read process Rp, always following the write process Wp, begins by removing the frame F element from the initial fixed memory stack location. The read process Rp then continues to remove frame F elements at sequential memory locations by incrementing the read pointer Rptr at a rate indicated by the local clock Lclk. When the end of the data frame F has been reached the read process Rp will continue to read from the stack MS and pass invalid information to the next data processing stage DP of the telecommunications network node TNN. This data however, will be discarded at the processing stage DP. When the pointer synchronization circuit PSC detects the beginning of a new frame F input, that is, the bit synchronization field BSy of the data frame F, it will set, by means of a set command SRc and a read address set signal SRptr, the read pointer Rptr to the same fixed initial value used for the write pointer Wptr.

The described process is repeated continuously for every frame F input.

It has to be noted that here the pointer synchronization controller PSC is not necessarily limited to detecting the specific fields mentioned above. It is also understood that it could be implemented in such a flexible manner so that any data string combination is recognized.

Also, it is worth to mention that in some cases it is advantageous to integrate the bit rate adaptation function BAS into a Clock and Data Recovery system or into a memory unit circuit.